An Ultra-Low Power Multi-Level Power-on Reset for Fine-Grained Power Management Strategies

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***Abstract*—This paper proposes a multi-level POR circuit with programmable voltage thresholds, that can operate in different fine-grained power management strategies. The POR is designed in a 0.18μm standard-logic CMOS technology, and occupies an area of 110μm x 70μm. Simulations results show a robust performance over process and temperature variations (PVT), rising times ranging from 1μs to 1s, and different supply values, while consuming a current of 19nA.**

***Index Terms*—Power-on Reset (POR), fine-grained, power management, delay adjustable, multiple threshold, power-on detection, supply monitoring, ultra-low power.**

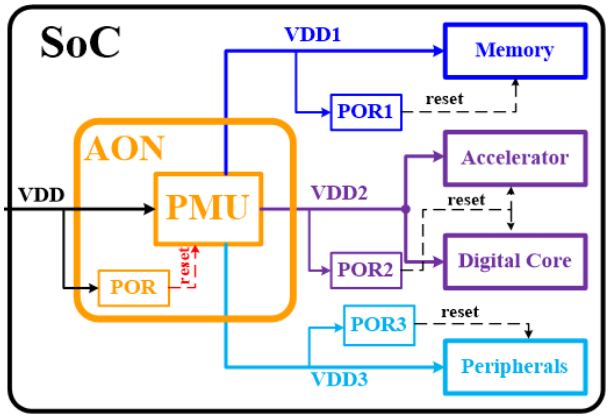
I. Introduction

Fine-grained power management is becoming an attractive approach in energy-autonomous and battery supplied applications at the edge of Internet-of-Things (IoT). Power Management Units (PMUs) control how energy is administered in a System-on-Chip (SoC). Figure 1(a) shows a fine-grained PMU scheme. To save energy, the PMU can command the memory, digital core, accelerators and peripherals into idle and sleep states. Power supply is restored by re-enabling individual voltage regulators. The supply voltages are usually constrained to the lowest operational level of the domain without impacting the robustness of its blocks. Upon request, the blocks can be turned-on, individually, through power gating.

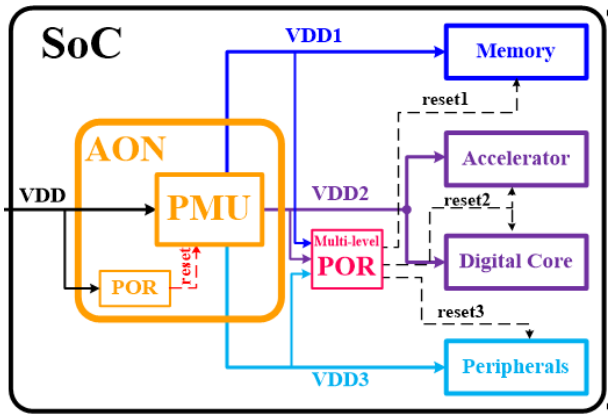
In spite of the efforts to implement such power-up schemes to ease load regulation, individual domains might still suffer from local regulator settling time. Restoring supply from local regulators require a finite time to reach steady nominal voltage. During the ramp-up of a local supply, memory and registers might have floating states causing undesired initial behavior [1]. To avoid this situation, a common solution is to hold the circuit into a reset state until the local regulator reaches a level that guarantees correct operation. This task is performed by a power-on reset (POR) circuit.

Traditional POR circuits are designed with a fixed threshold level detection, forcing to design and place a different POR for each domain [1]–[3]. Implementation of a single POR circuit for each voltage domain increases design area, cost (considering its re-design to adjust the threshold level), and power consumption.

This work presents an improved version of the circuit presented in [4], based on a multilevel approach. The proposed POR is capable of tracking supply ramps ranging from 1μs to 1s, while consuming 2 order of magnitude less than its predecessor.



(a) Locally distributed POR strategy.



(b) Global POR strategy

Fig. 1. POR strategies for SoC with multiple supply voltage domains.

II. Multilevel POR Circuit

A. Fine-Grained PMU Strategies

Fine-grained power management generally adopts a locally-distributed PMU-POR strategy as Figure 1(a) shows. The aim is to supply, in an efficient way, every voltage domain sub-systems. Once the global POR ensures a safe start-up of the chip, the PMU provides activation signals for local regulators. The local PORs will then guarantee risk-free turn-on conditions in every domain. The advantage of such scheme is the possibility to turn-on multiple domains simultaneously. The obvious disadvantages are larger design area, current consumption, and design cost.

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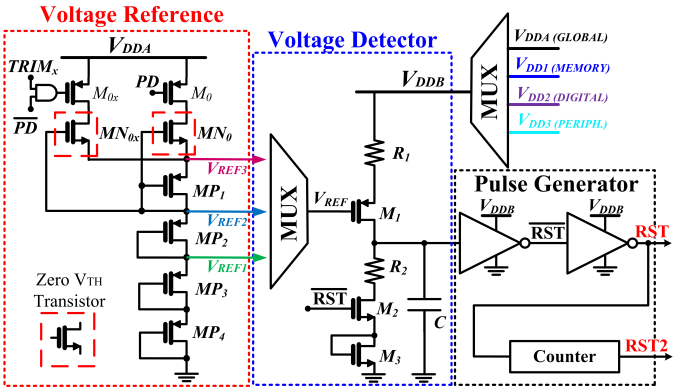


Fig. 2. Proposed POR circuit.

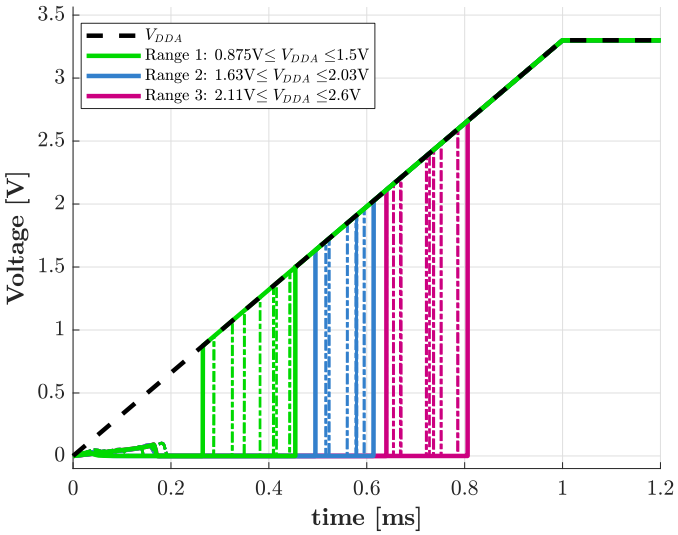


Fig. 3. POR signals over PVT variations for V_{DDA} ramp of 1ms ($V_{DDB} = V_{DDA}$).

To solve these problems, a modular approach can be implemented. As an example, the POR in [4] consists of a voltage reference, a voltage detector, and a pulse generator. Instead of placing the entire POR cell to check the target supply, only the voltage detector can be used. At the same time, all the local PORs can reuse the voltage reference block. As a result, low power, reduced area and design costs are possible.

Another possible option for power, area, and cost optimization is to use a single POR, as shown in Figure 1(b). In that case, an additional mux is required to select the target supply voltage. Requirements in a PMU with only one POR circuit imply multiple operation levels. Considering the PMU is in the always-on domain, every time a sub-system is turned-on, the global POR is set to the appropriate voltage threshold. Then, this POR checks the start-up of every domain at a time, in a sequential manner. The disadvantage of such a scheme lies in the inability of power-up different domains at the same time.

The main idea of this work is to introduce a circuit that can be used in either of the PMU strategies discussed. The following section, describes the proposed topology.

B. Proposed circuit description

This section presents the proposed POR, and the improvements made over the circuit presented in [4]. With this modifications, current consumption on the order of nano-amperes, and a wide range of supply rising times are possible.

The proposed POR is a modular circuit composed by three functional blocks as shown in Figure 2. The first block is an adjustable voltage reference, which allows the generation of multiple POR thresholds. This block is exactly the same one implemented in [4], based on the sub-threshold reference proposed in [5]. No further description of this circuit will be presented. The second block, the voltage detector, monitors the supply voltage V_{DDB} and generates a delayed signal that goes to the third block. Finally, the pulse generator sets a logic one, once the capacitor voltage crosses a certain threshold voltage. As an option, the *RST* signal can drive a counter. The latter provides the possibility of controlling the reset delay time. This feature is useful when circuits, such as oscillators, need a longer time to settled.

At the beginning of operation, when the supply voltage V_{DDB} starts to ramp-up, transistor M_1 remains off and the capacitor is discharged. When $V_{DDB} = V_{REF}$, M_1 is in weak inversion, and the low current starts to charge capacitor C. It is not until $V_{DDB} = V_{REF} + |V_{thp}|$ that M_1 enters strong inversion, forcing a greater current to charge the capacitor. This charge time depends on the slope of the V_{DDB} ramp, limited by the difference between the current supplied by M_1 and the current sinked through the branch formed by R_2 and M_3. In other words, for fast ramps, the time constant of the voltage detector limits the response. Once the voltage at the capacitor reaches the pulse generator input threshold, the POR signal (*RST*) is triggered.

The main difference of this POR with respect to the one presented in [4] lies in the voltage detector. When the threshold of the pulse generator is reached, the signal $\overline{RST}$ turns off transistor M_2, forcing C to charge completely up to V_{DDB}. Turning-off M_2 means reducing the quiescent current of the block to the order of nano-amperes.

The other noticeable change is the input block of the pulse generator, which in [4] is a schmitt trigger. The purpose of the schmitt trigger was establishing a different threshold for a brown-out (BO) event. This is not longer needed, since the voltage detector performs this function as well. In the presence of a BO event, the capacitor voltage tries to follow V_{DDB}.[1] It is not until V_{DDB} is close to V_{REF} (which is below the POR threshold), that the voltage at the capacitor starts to differ from V_{DDB}, since M_1 turns completely off. At this point the voltage capacitor is set to the voltage divider formed by two high

[1]This condition is restricted by the time constant formed by R_1 and C (which filters short duration BO event).

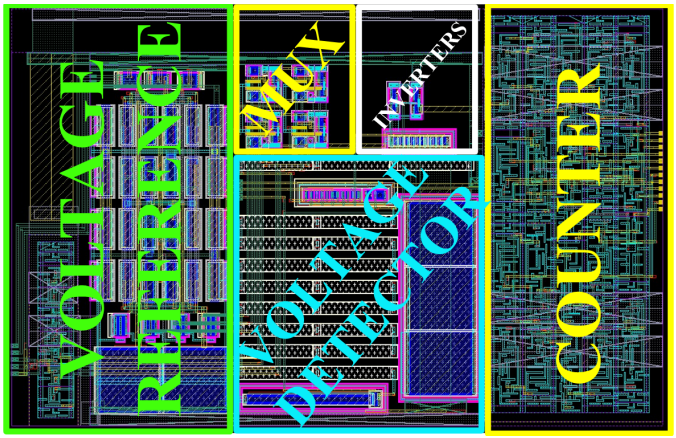


Fig. 4. Layout of the proposed POR (area of $110\mu m$ x $70\mu m$).

impedance branches (M_1-R_1, and M_2-M_3-R_2). As the voltage capacitor gets lower than V_{DDB}, $\overline{RST}$ starts to rise-up, turning M_2 on, until the point the capacitor is completely discharged, setting $\overline{RST}$ as a logic one.

Figure 3 shows the the RST signal behavior for the case of a global POR ($V_{DDA} = V_{DDB}$, chip turn-on condition) over PVT variations, with a 1ms ramp. In this graph, three distinguishable ranges can be seen, which correspond to the different V_{REF} levels. In order to show the robustness of the circuit, the following section will present and discuss the results obtained.

III. Results

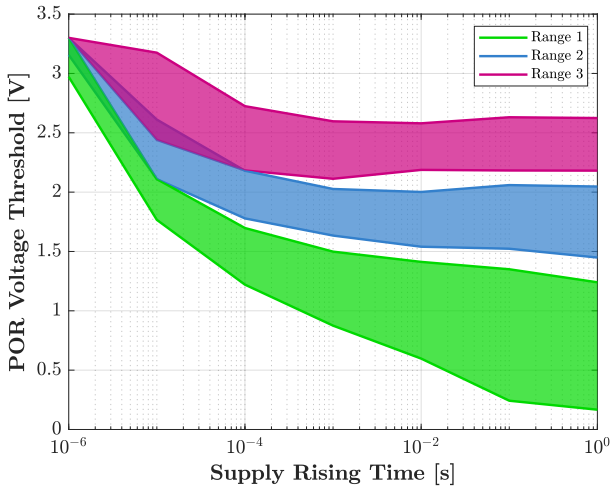
The POR circuit was implemented in a TSMC $0.18\mu m$ standard-logic CMOS technology, occupying an area of $110\mu m$ x $70\mu m$. The nominal power supply is 3.3V, which corresponds to the I/O supply of the used technology. Fig. 4 shows the layout of the proposed circuit. This section discusses the test conditions used for circuit validation, as well as the obtained results. Finally, the performance of the proposed POR is compared with state-of-art POR circuits.

During the chip (global) or local power-up, the supply signal ramp could have different rising times. The latter dependes on the physical and factory characteristics of the battery, or in the case of the local regulator, its dynamic behavior. For this reason, in order to test the POR circuit, two different scenarios are simulated: one for a global POR, and one for a local POR.

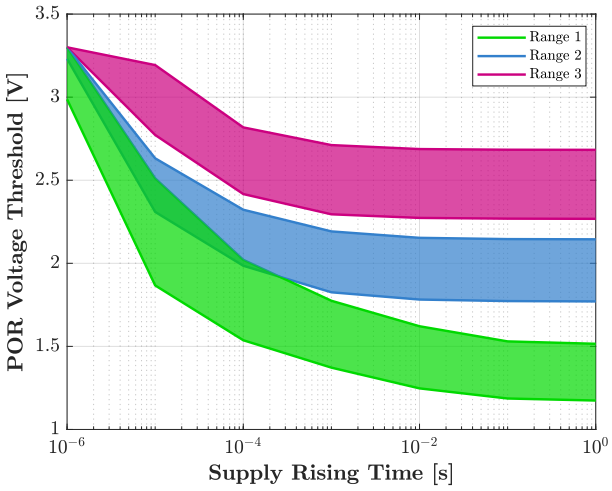
In Figure 5, the reset threshold voltages for different supply ramps can be appreciated. In these two plots, three different ranges are distinguishable within each color region. [2] These ranges appear when the three different V_{REF} levels are applied. Furthermore, with these plots, the aforementioned scenarios can be analyzed.

Figure 5(a) shows the results for the global POR, or chip turn-on condition. In this case, the supplies of the reference voltage (V_{DDA}) and the rest of the circuitry (V_{DDB}) are the same. The first thing to notice is that, for fast ramps (i.e, lower

[2]All corner cases are within these regions.



(a) Global POR.



(b) Local POR.

Fig. 5. POR voltage thresholds ranges for different supply ramps over PVT variations, and for a supply voltage of 3.3V. The green, blue and magenta regions, show the upper and lower limits of the different threshold voltage ranges when using V_{REF1}, V_{REF2} and V_{REF3} as the reference, respectively (see Figure 2).

than 1ms), the threshold voltages for the three ranges are 3.3V, or close to that value. The reader might be tempted to conclude that, once the supply reach this value the reset is triggered. In fact, the voltage detector starts to charge the capacitor at the same level as for slow cases ($V_{DDA} = V_{REF} + |V_{thp}|$), but the response is limited by the time constant of the voltage detector. Then, it will require extra time before the capacitor reaches a value to trigger a reset signal. The second thing to observe appears for ramps slower than 100us; for ranges 2 and 3, the maximum and minimum stabilize to constant values. Meanwhile, for range 1, the lower limit diminish with slower ramps. The reason is because V_{REF} is also in a turn-on condition and its value, at the trigger moment, has not settled. This is even more critical for the lowest level V_{REF1}, as V_{sg1} (in Figure 2) will be sufficient to charge the capacitor at lower

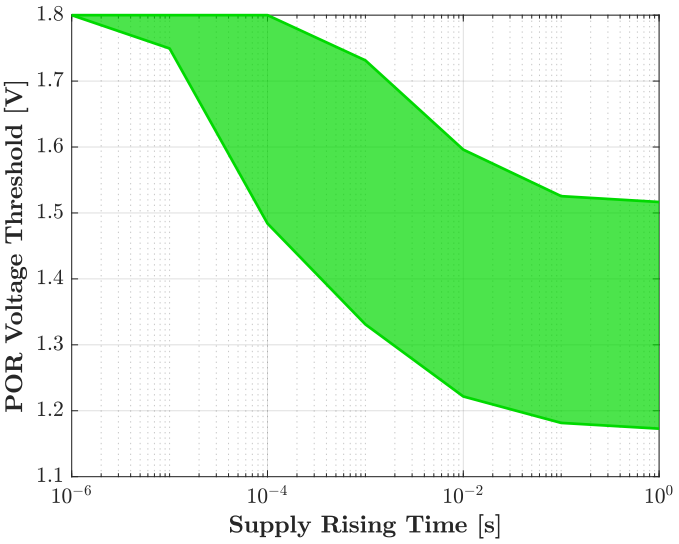


Fig. 6. POR voltage threshold, for different supply ramps over PVT variations, and for a local supply voltage of 1.8V. As expected, only reset signals are present for range 1.

values of the supply voltage. This design was aimed for a top level supply voltage of 3.3V, so range 2 and 3 are enough. Even more, they behave as expected with slow ramps, which is in fact, the usual condition for the global POR.

Figure 5(b) shows the results for the local POR, or local regulator power-up. In this case, the supply of the reference voltage is the global one (V_{DDA} already settled), and the local supply (V_{DDB}) are different. The behavior is very similar to global POR case. The difference are in the limits values, which are much better behaved for all three ranges. This was expected, since this case uses a steady reference, in contrast with the global case.

It is worthwhile to investigate what happens when the local supply is not 3.3V, but lower than this value (as it would be the case). Figure 6 shows the different POR voltage thresholds with a local supply of 1.8V, against different supply ramps. It can be seen that the reset is only triggered for V_{REF1}, since the other ranges are well above the 1.8V supply value. It is important to mention that for fast rising times, the reset signal will take longer to trigger (e.g., for a ramp of 1us, the worst-case triggers a reset at 41us). This happens because V_{sg1} will not be as high as for the 3.3V case. If the application demands it, two strategies to allow faster responses can be implemented: change M_1 for a lower V_{th} transistor, or use a smaller charging capacitor.

Table I shows the performance summary. The circuit was validated for the industrial temperature range (from -40°C to 120°C) and for all process corners. The POR offers three different reset voltage thresholds according with the chosen V_{REF}. The quiescent current is around 19nA for typical case. It has a maximum current consumption of 1.2μA, and is caused by the voltage reference block, in a fast corner. Finally, Table I compare the performance of the proposed POR with state-of-art architectures.

TABLE I
COMPARISON WITH PRIOR WORK AND RESULTS SUMMARY.

	[6]	[7]	[1]	[4]	This work
Technology	0.5um	0.5um	180nm	180nm	180nm
Supply Voltage [V]	1.2-3.3	1.8-5.5	1.8	1.8-3.3	1.8-3.3
Current [nA]	76	N.A.	1000	7000	**19**
PO rise time [ms]	<10	<1	**<1000**	<50	**<1000**
Temperature [°C]	–	**-40 - 125**	-20 - 100	**-40 - 125**	**-40 - 125**
Multi-Level	**Yes**	No	No	**Yes**	**Yes**
Area [um^2]	**1900**	27000	12000	5700[a]	5700[a]

Results Summary						
VDD Ramp	**1us**		**1ms**		**1000ms**	
POR case	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**
Range1 [V][b]	1.8	1.8	1.33	1.73	1.17	1.52
Range2 [V][b,c]	2.5	2.5	1.63	2.03	1.45	2.05
Range3 [V][c]	3.3	3.3	2.11	2.6	2.18	2.62

	Min.	**Typ.**	**Max.**
Current [nA]	0.12	19.17	1222

[a] Area excluding the counter.
[b] Limits for Local POR case ($V_{DDB} = 1.8V$ or $2.5V$).
[c] Limits for Global POR case ($V_{DDB} = 3.3V$).

IV. SUMMARY

In this paper, an ultra-low power multi-level POR circuit, that can be implemented in different fine-grained power management schemes is presented. Simulation results over PVT variations, and a wide supply rise times, ranging from 1us to 1s, show a robust performance within the industrial temperature range from -40°C to 125°C. The POR has a nominal current consumption of 19nA, and can enable up to 3 different POR levels for different SoC applications. Current consumption, programmability, and reduced area, makes this circuit an attractive solution for ultra-low power SoC applications.

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